九齊科技股份有限公司
Nyquest Technology Co., Ltd.

DATA SHEET

NY8L020A

8-bit 65C02 MCU with 8x31 LCD Driver, 20 I/O, & Buzzer Output

Version 1.0

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Revision History

Version	*Date*	*Description*	*Modified Page*
1.0	2018/10/12	Formal release.	-

1. 概述

NY8L020A 爲高性能 8 位元 65C02 微控制器附加LCD驅動和Buzzer播放功能，三組8位元 timer / counter，20根I/O。LCD 驅動單元除控制面板功能之外，還內建按鍵偵測功能。

MCU 為 CISC 架構易於編程和控制以及規劃到多種的應用。此外並提供多種工作模式 Slow mode、Standby mode 及 Halt mode (Sleep Mode) 來有效減少功耗。

2. 功能

- 寬廣的工作電壓範圍：1.1V~3.6V @ System clock ≤ 500KHz；2.0V~3.6V @ System clock ≤ 4MHz。
- 16K-Byte ROM。
- 128-Byte RAM。
- LCD 點數 (COM x SEG)：8 x 31。
- 20 GPIO，其中 10 根和 LCD SEG 共用。
- 雙時脈振盪：系統時鐘可自由選擇高速或低速。
  - 高速振盪: IOSC4M / IOSC2M / IOSC500K。
  - 低速振盪: IOSC32K / XTAL32K。
- 內建高精準振盪線路(+/- 1.5%)。
- 四種工作模式可有效省電減少功耗：
  - Normal mode、Slow mode、Standby mode 及 Halt mode。
- Normal mode 下 CPU clock 速度可程式化：
  - 可設定為高速振盪的 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128。
- 3 組 8 位元 Timer，可應用於1通道或2通道Buzzer或 RFC 等等應用。
- 支援大多數 LCD 顯示：
  - 1/2, 1/3 bias。
  - 1/2, 1/3, 1/4, 1/5, 1/6, 1/8 duty。
- 內建 Charge pump 昇壓供應 LCD 顯示。
- COM & SEG 可設定成 LED sink / drive 功能。
- LCD 支援 Matrix key 功能，input & output 起始位置可在組態中設定。
- Serial peripheral interface (SPI) Master mode 可存取 SPI 元件。
- EL 驅動功能，可設定頻率和佔空比。
- RFC 功能，可用於温度、濕度偵測應用。
- 完整的系統保護，Watch-dog reset 看門狗重置功能及external reset pin 外部重置腳。
- 彈性化的 I/Os 設定：floating 輸入、pull-low 輸入、CMOS 輸出、open-drain 輸出。

- 紅外線載波頻率可供選擇，同時載波之極性也可以根據數據作選擇。
- 1 或 2 通道Buzzer。
- 7 種中斷模式。
- LCD 點數組合：

COMMON	SEGMENT	DOTS
8	31	248
6	33	198
5	34	170
4	35	140
3	36	108
2	37	74

1. GENERAL DESCRIPTION

NY8L020A is a high-performance 8-bit 65C02 micro-controller with LCD driver and buzzer output, three sets of 8-bit timer/counter, 20 general I/Os. For LCD driver, it applies for the most common-used LCD panels and functions as a key strobe for further application.

The CISC MCU architecture is very easy to program and control, various applications can be easily implemented. Furthermore, in addition to the Slow mode, it offers the Standby mode and Halt mode (Sleep mode) to minimize power dissipation.

2. FEATURES

- Wide operating voltage range: 1.1V ~ 3.6V @ System clock ≤ 500KHz; 2.0V ~ 3.6V @ System clock ≤ 4MHz.
- 16KB ROM.
- 128B RAM.
- LCD Dots (COM x SEG): 8 x 31.
- 20 GPIO, 10 shared from LCD SEG.
- Dual-clock oscillation: System clock can switch between high oscillation and low oscillation.
  - High oscillation: IOSC4M / IOSC2M / IOSC500K.
  - Low oscillation: IOSC32K / XTAL32K.
- Precisely embedded oscillator with build-in resistor (+/- 1.5%).
- Four kinds of operation mode to reduce system power consumption:
  - Normal mode, Slow mode, Standby mode and Halt mode.
- At Normal mode, CPU clock is software programmable.
  - 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 of high oscillator (F_{FAOS}) frequency.
- Three 8-bit timers for 1-channel or 2-channel buzzer or other applications such as RFC.
- Support most of LCD panel types:
  - 1/2, 1/3 bias.
  - 1/2, 1/3, 1/4, 1/5, 1/6, 1/8 duty.
- Charge pump for the LCD display power.
- LED sink/drive configuration supported through COM & SEG.
- Matrix key supported, and input & output starting pad can be selected by option.
- Serial peripheral interface (SPI) Master mode for serial Flash/SRAM memory.
- EL driver block supported with various frequency and duty.
- RFC-functioned block for the detection of humidity, temperature or other applications.

- Low voltage reset, watch-dog reset (by option) and external reset pin (by option) are all supported to protect the system.
- Flexible I/Os maximum with optional function: floating input, pull-low input, CMOS output, open-drain output.
- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.
- 1-channel or 2-channel buzzer
- 7 interrupt modes supported.
- Possible LCD COM and SEG combination:

COMMON	SEGMENT	DOTS
8	31	248
6	33	198
5	34	170
4	35	140
3	36	108
2	37	74

3. BLOCK DIAGRAM

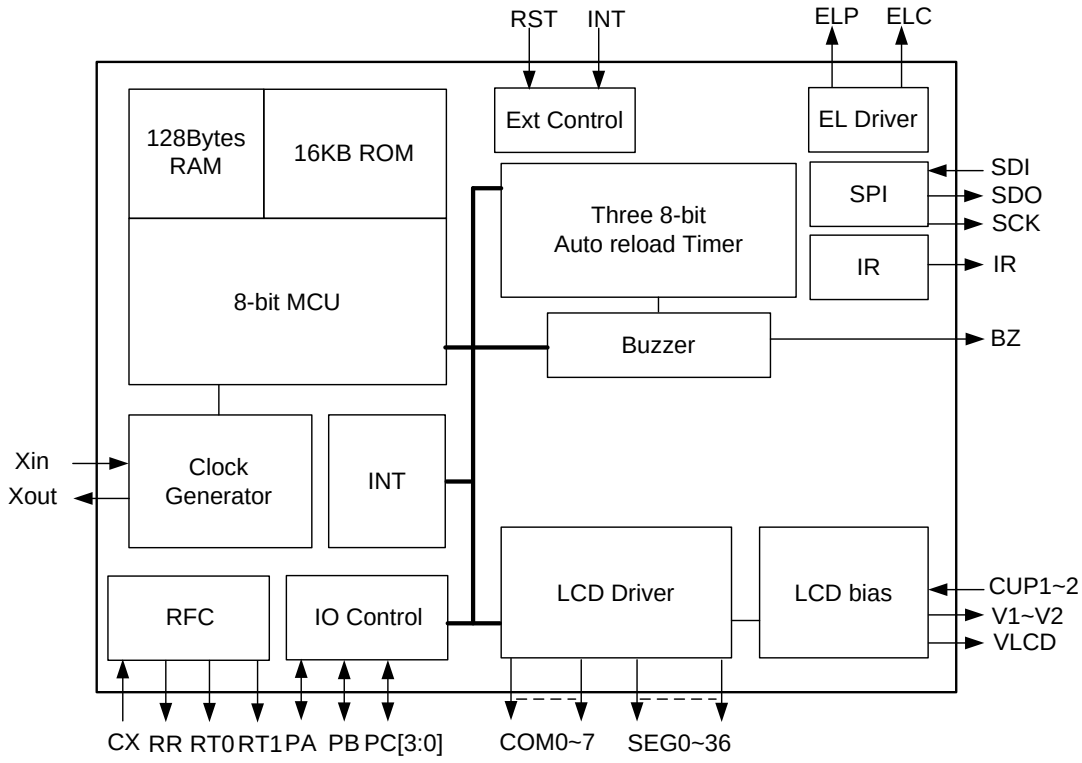

Fig.1-1: The block diagram

4. PAD DESCRIPTION

Pad Name	ATTR.	Description
VDD	P	Positive supply power.
VSS	P	Negative supply power.
PA0/Xin	I/O	Bit 0 for Port A, or input of XTAL32K.
PA1/Xout	I/O	Bit 1 for Port A, or output of XTAL32K.
PA2/INT	I/O	Bit 2 for Port A, or external interrupt input.
PA3/RST	I/O	Bit 3 for Port A, or external reset input.
PA4/CX	I/O	Bit 4 for Port A, or input of RFC function.
PA5/RR	I/O	Bit 5 for Port A, or output of RFC function.
PA6/RT0	I/O	Bit 6 for Port A, or output of RFC function.
PA7/RT1	I/O	Bit 7 for Port A, or output of RFC function.
PB0/BZ	I/O	Bit 0 for Port B, or buzzer output.
PB1	I/O	Bit 1 for Port B.
SEG0/PB2/ELP	I/O	LCD segment 0, Bit 2 for Port B, or charging signal of EL driver.
SEG1/PB3/ELC	I/O	LCD segment 1, Bit 3 for Port B, or discharging signal of EL driver.
SEG2/PB4/IR	I/O	LCD segment 2, Bit 4 for Port B, or IR output.
SEG3/PB5/SCK	I/O	LCD segment 3, Bit 5 for Port B, or clock output of SPI.
SEG4/PB6/SDI	I/O	LCD segment 4, Bit 6 for Port B, or data input (MISO) of SPI.
SEG5/PB7/SDO	I/O	LCD segment 5, Bit 7 for Port B, or data output (MOSI) of SPI.
SEG6~9/PC0~3	I/O	LCD segment 6~9, or Bit 0~3 for Port C (can be used as key strobe input).
SEG10~30	O	LCD segment 10~30 (SEG10~25 can be used as key strobe output).
COM0~7	O	LCD common 0~7 (COM2~7 can be used as SEG36~31).
V1~2, VLCD	P	LCD supply power.
CUP1~2	I/O	Auxiliary capacitor pins for voltage pumping.

Total：57 Pins

Legend: I = Input O = Output P = Power

5. OPERATION MODES

NY8L020A provide four kinds of operating mode to tailor all kinds of application and save power consumptions. These operating modes are Normal mode, Slow mode, Standby mode and Halt mode. Normal mode is designated for high-speed operating mode. Slow mode is designated for low-speed mode in order to save power consumption. At Standby mode, NY8L020A will stop almost all operations except Timer2/ Timer1/Timer0/FT/ST (based on F_{SLOW}) in order to wake up periodically. At Halt mode, NY8L020A will sleep until Key change or external interrupt occurs. User can set the control register OPMD to swap Normal/Slow mode and the control register SLP to enter Standby/Halt mode.

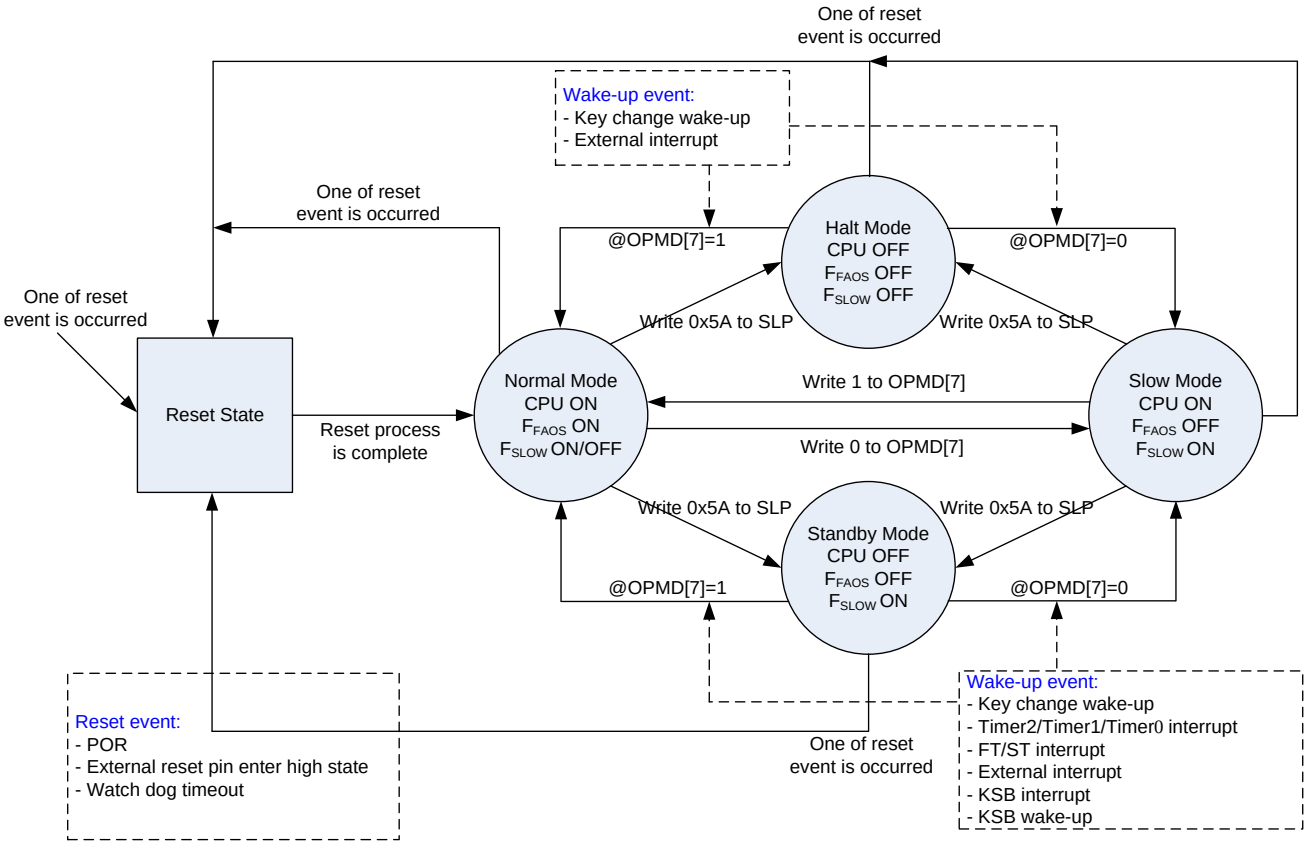

Fig. 5-1: Four Operating Modes

6. LCD WAVEFORMS

The following lists voltage level of corresponding bias settings and users have to connect with the identical power system.

Bias	Voltage Level
1/2	VSS, V1 (1/2*VLCD), VLCD
1/3	VSS, V1 (1/3*VLCD), V2 (2/3*VLCD), VLCD

The LCD timing waveforms are shown as Fig.6-1 ~ Fig.6-2.

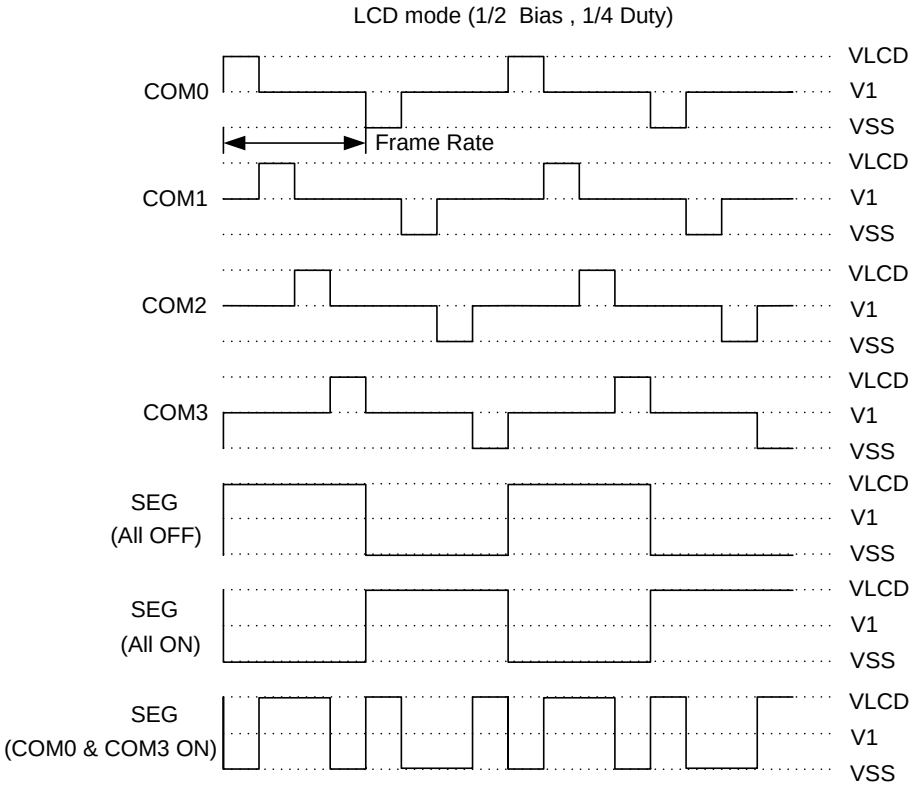

Fig.6-1: LCD timing waveform of 1/2 bias, 1/4 Duty

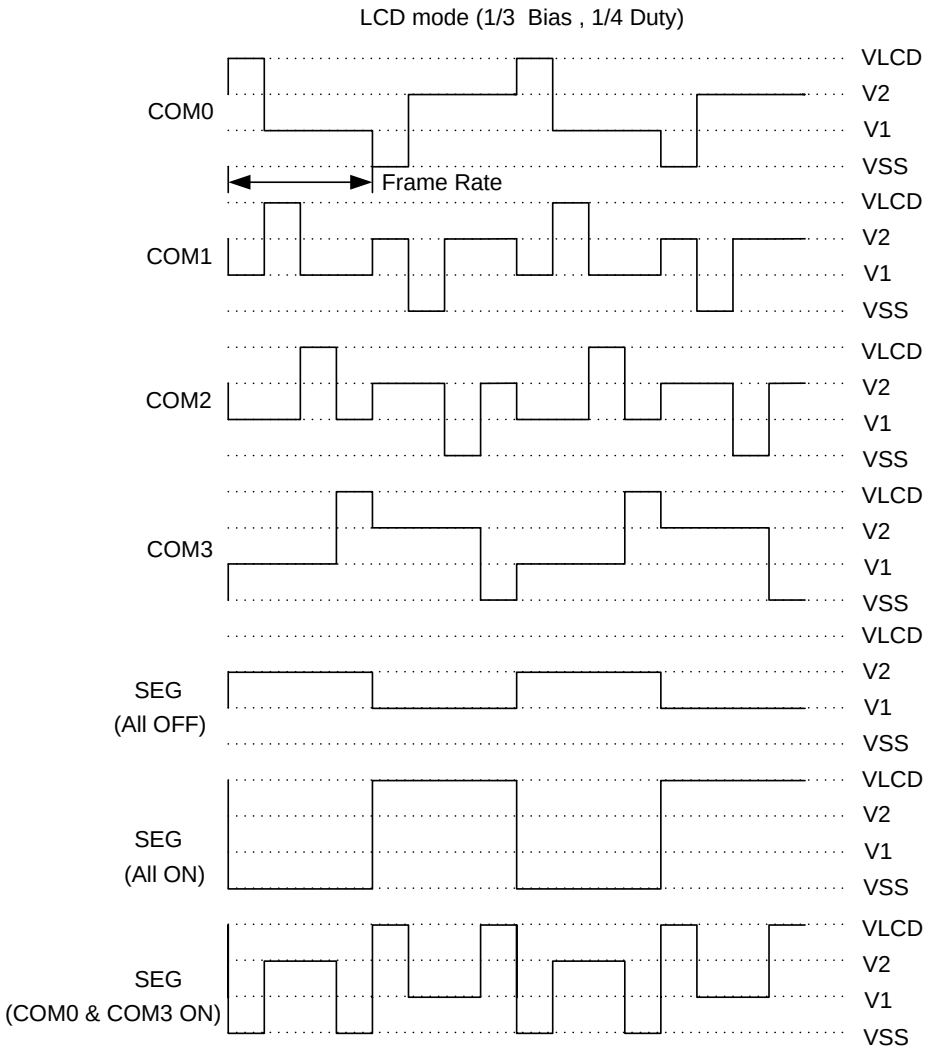

Fig.6-2: LCD timing waveform of 1/3 bias, 1/4 Duty

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
VDD - VSS	Supply voltage	-0.5 ~ +4.0	V
Vin	Input voltage	VSS–0.3V ~ VDD+0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

7.2 DC Characteristics

Symbol	Parameter		VDD	Min.	Typ.	Max.	Unit	Test Condition
V_{DD}	Operating voltage			1.1	1.5	3.6	V	F_{CPU} = 500KHz
				2.0	3	3.6		F_{CPU} = 4MHz
I_{HALT}	Supply Current	Halt mode	1.5		0.1	0.5	uA	Sleep, no load
			3		0.1	0.5		
I_{SB1}		Standby mode1	1.5		1.3		uA	CPU off, IOSC32KHz on, LCD off, Reg off, no load
			3		2.2			
I_{SB2}		Standby mode2	1.5		1.4		uA	CPU off, IOSC32KHz on, LCD on, Reg off, no load
			3		2.3			
I_{SB3}		Standby mode3	1.5		3.8		uA	CPU off, IOSC32KHz on, LCD on, Reg on, no load
			3		5			
I_{SL}		Slow mode	1.5		6		uA	F_{CPU} = IOSC32KHz, no load
			3		20			
I_{OP}		Normal mode	1.5		90		uA	F_{CPU} = 500KHz, no load
			3		300			
			3		1.0		mA	F_{CPU} = 4MHz, no load
I_{IH}	Input current (Internal pull-low)	Weak (1M ohms)	1.5		0.5		uA	V_{IN} = VDD
			3		3			
		Strong (100K ohms)	1.5		5			
			3		30			
I_{OH}	Output high current (PA/B/C, SEG/COM@LED mode)		1.5		-2		mA	V_{OH} = 1.0V
			3		-9			V_{OH} = 2.0V
I_{OL1}	Output low current (PA/B/C)		1.5		4		mA	V_{OL} = 0.5V
			3		18			V_{OL} = 1.0V
I_{OL2}	Output low current (SEG/COM@LED mode)		1.5		2		mA	V_{OL} = 0.5V
			3		9			V_{OL} = 1.0V
ΔF/F	Frequency deviation by voltage drop(500KHz)		1.5		-0.5		%	$\frac{Fosc(1.5V) - Fosc(1.2V)}{Fosc(1.5v)}$
	Frequency deviation by voltage drop(4MHz)		3		-0.5			$\frac{Fosc(3.0V) - Fosc(2.4V)}{Fosc(3.0v)}$
ΔF/F	Frequency lot deviation (500KHz)		1.5	-1.5		1.5	%	$\frac{Fosc(1.5V) - 500KHz}{500KHz}$
	Frequency lot deviation (4MHz)		3	-1.5		1.5	%	$\frac{Fosc(3.0v) - 4MHz}{4MHz}$

Symbol	Parameter	VDD	Min.	Typ.	Max.	Unit	Test Condition
Fosc	Oscillation Frequency	--	0.48	0.5	0.52	MHz	V_{DD} = 1.1~3.6V
			1.95	2	2.05		
			3.9	4	4.1		

8. APPLICATION CIRCUITS

8.1 Application Circuits with Low Loading

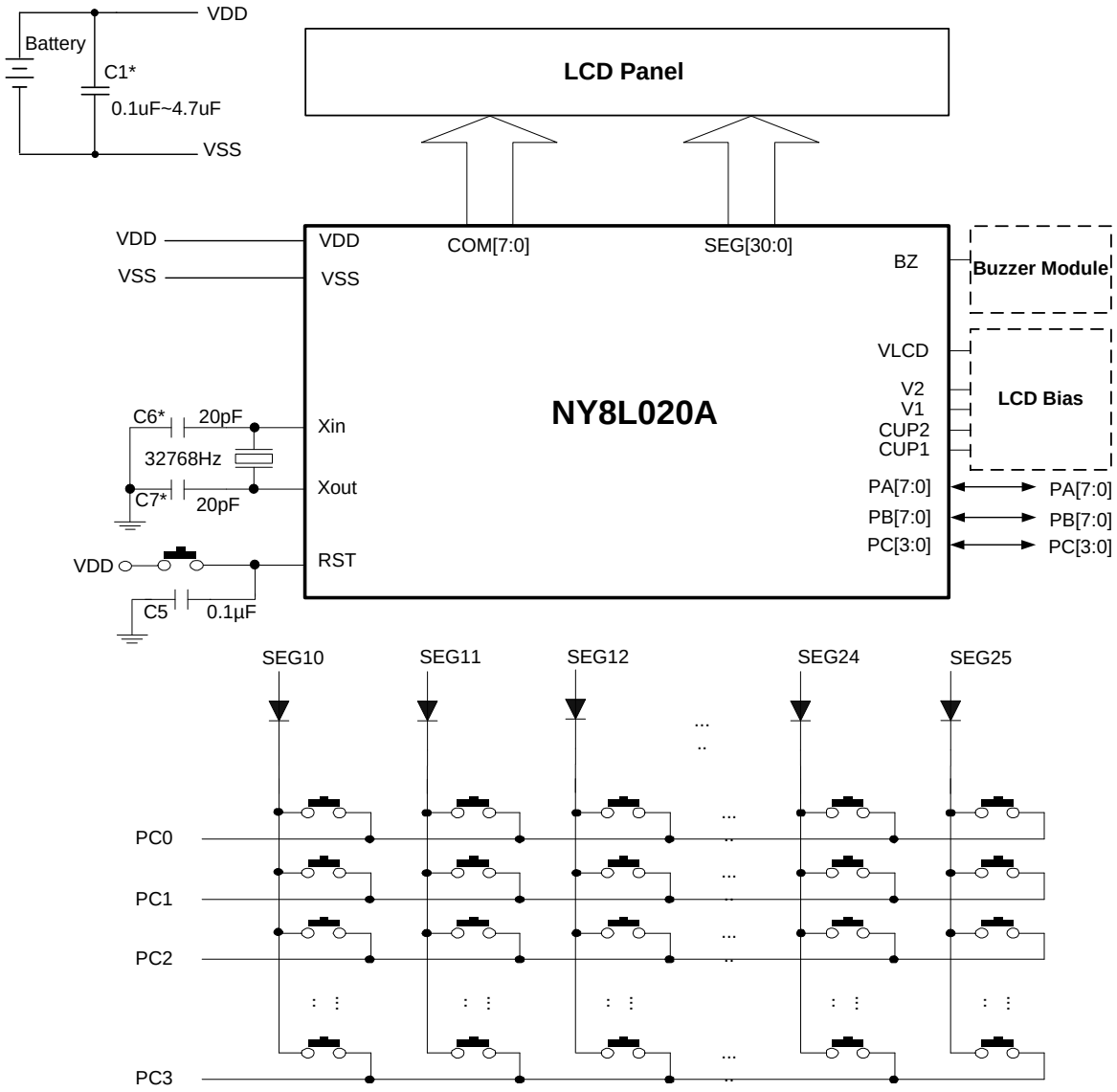

Fig.8-1: The Application Circuits with Low Loading

PCB Layout Guidelines:

1. VDD must be connected to power input port directly, not the branch of each other.

2. VLCD should be higher than or equal to VDD, otherwise will cause large current.

3. VSS must be connected to ground input directly, not the branch of each other.

4. Capacitor (used for XTAL32K) is proposed to be 12~20 pF.

5. C1 is suggested 0.1uF~4.7uF.

8.2 LCD Bias (VDD for VLCD/V2/V1 or internal Vreg for V1)

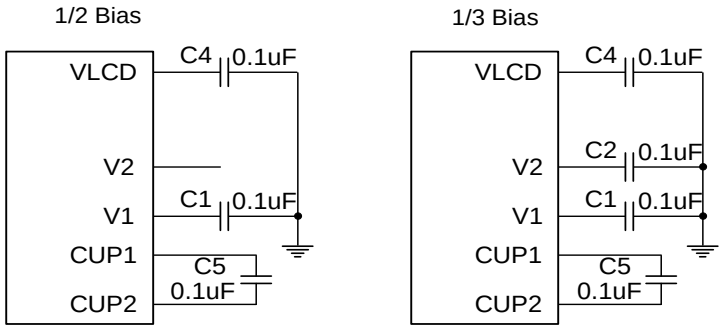

Fig.8-2: The diagram of LCD Bias based on VDD or internal Vreg

9. DIE PAD DIAGRAM